BEE 271 Final exam, Spring 2017

Full name: _____

This exam is closed book, closed notes, no cellphones or computers and unproctored. Please try sit next to students you don't normally. You may take this exam to another room if you would be more comfortable. You have 2 hours to answer as many questions as you can. Some questions are easy and some are hard but each is worth the same 5 points, so pick and choose. Most correct answers can be fairly short. If you need more space, additional sheets may be stapled to your exam. I will be outside the room if you need to discuss something.

Please copy the following statement *in your own handwriting* and s*ign your name* below it:

> On my honor, I will neither accept nor give unauthorized aid on this exam.
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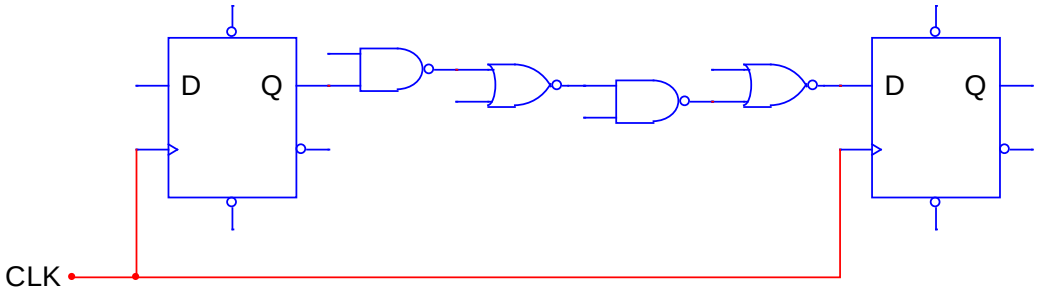
> Signed

1. What are t_{su}, t_h and t_{cQ}? Draw a diagram showing how they're measured.

2. Draw a circuit for a gated latch using NAND gates.

3. Referring to the following circuit fragment, assume this represents the critical path in an actual circuit where the rest of the pins have sensible inputs and that t_{su} = 0.3 ns, t_h = 0.2 ns, 0.5 ns ≤ t_{cQ} ≤ 0.6 ns and t_{gate} = 0.4 ns. What is f_{max}?



4. What do the terms, edge-triggered and active edge mean?

5. You are to write a Verilog module called Digit that implements one digit decimal counter (one that counts 0 to 9). It should have a synchronous reset and enable plus a special feature: It should tell you when it's about to rollover so that it can be used to build this 4-digit counter:

```
module FourDigits( input clock, reset, enable,
      output [ 3:0 ] bcd[ 3:0 ] );
   wire [ 5:0 ] ro;
   Digit d0( clock, reset, enable,  bcd[ 0 ], ro[ 0 ] );
   Digit d1( clock, reset, ro[ 0 ], bcd[ 1 ], ro[ 1 ] );
   Digit d2( clock, reset, ro[ 1 ], bcd[ 2 ], ro[ 2 ] );
   Digit d3( clock, reset, ro[ 2 ], bcd[ 3 ], ro[ 3 ] );
endmodule
```

Here's the interface to the module you should write. Please write the rest.

```
module Digit( input clock, reset, enable,
      output reg [ 3:0 ] digit,
      output rollover );
```

6. What is the difference between a latch, a gated latch, a master-slave flip-flop and an edge-triggered flip-flop? Draw schematic symbols for each.

7. Design a 3-bit one-hot counter in Verilog with an asynchronous reset.

8. Write a Verilog module that implements a D flip-flop with a synchronous reset.

9. Write a Verilog module that implements a JK flip-flop with an asynchronous reset.

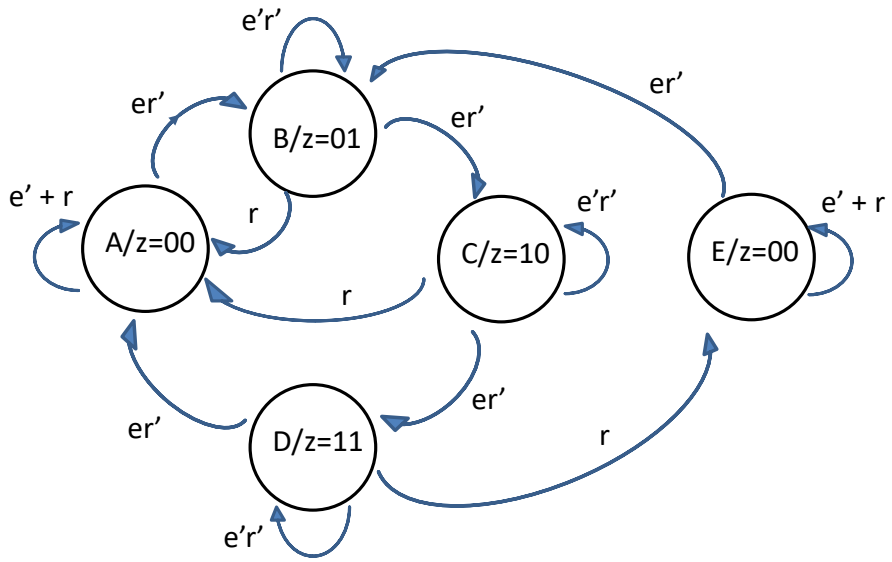
10. What does FSM stand for? Why are sequential circuits called FSMs? (What is the significance of the "FS" part?)

11. For two states to be equivalent, what has to be true about them?

12. What is the difference between a Mealy and a Moore design? Draw a picture of each.

13. How would you decide whether to use a Moore versus a Mealy design? Which one typically produces outputs one clock sooner?

14. The next several questions relate to this FSM. You may assume a clock. First, is this a Mealy or a Moore machine?



15. Create a state table for this FSM.

16. Find any equivalent states by partitioning, first by output, then by successors.

17. Create a minimized state table eliminating any equivalent states you discovered.

18. Create a state diagram for your minimized FSM or mark your changes on the original diagram.

19. Write a Verilog module that implements your minimized FSM.

20. Create a 3-bit counter in Verilog that cycles through this sequence, 6, 2, 4, 5, 0, 7, 3, 1, with a synchronous reset to 4.